implanting an impurity into one region of the semiconductor adjacent to the member by ion irradiation with the member and a mask material as masks;

removing the mask material; and

doping another region of the semiconductor located adjacent to the member and opposite to the one region with an impurity having one conductivity type to form the another region to a depth shallower than that of the one region.

22. The method of claim 21 wherein the member comprises a floating gate.

23. The method of claim 21 wherein the one region overlaps with the member more widely than the another region overlaps with the member.

24. The method of claim 21 wherein at least a side of the member comprises an anodic oxide of a gate electrode material of the member.

25. The method of claim 21 wherein said impurity is activated by an electric power.

26. A method for forming a memory comprising:

forming a gate member comprising a floating gate, a control gate and an oxide provided on surfaces of the floating gate and the control gate on a single crystal substrate;

implanting an impurity into one region of the substrate adjacent to the member by ion irradiation with the member and a mask material as masks;

removing the mask material; and

doping another region of the substrate located adjacent to the member and opposite to the one region with an impurity having one conductivity type, to form the another region to a depth shallower than that of the one region.

27. The method of claim 26 wherein the memory has a flash memory.

28. The method of claim 26 wherein the memory has an EPROM.

29. The method of claim 26 wherein the memory has an EEPROM.

30. The method of claim 26 wherein the one region overlaps with the member more widely than the another region overlaps with the member.

31. A method for forming a memory comprising:

forming a gate electrode having a floating gate on a semiconductor;

forming a mask material on one region of the semiconductor;

introducing an impurity into another region of the semiconductor by ion implantation using the gate electrode and the mask material as masks;

removing the mask material; and

introducing the impurity into the one region, to form the one region to a depth shallower than that of the another region.

32. The method of claim 31 wherein the memory has a flash memory.

33. The method of claim 31 wherein the memory has an EPROM.

34. The method of claim 31 wherein the memory has an EEPROM.

35. The method of claim 31 wherein the one region has 0.1 μm or less in depth.

36. A method for forming a memory comprising:

forming a gate electrode having a floating gate on a semiconductor;

forming a mask material on one region of the semiconductor;

introducing an impurity into another region of the semiconductor by ion implantation using the gate electrode and the mask material as masks;

removing the mask material; and

introducing the impurity into the one region, to form the one region to a depth shallower than that of the another region,

wherein the another region overlaps with the gate electrode more widely than the one region overlaps with the gate electrode.

37. The method of claim 36 wherein the memory has a flash memory.

38. The method of claim 36 wherein the memory has an EPROM.

39. The method of claim 36 wherein the memory has an EEPROM.

40. The method of claim 36 wherein the one region has 0.1 μm or less in depth.

41. A method for forming a memory comprising:

forming a gate electrode having a floating gate on a semiconductor;

forming a mask material on one region of the semiconductor;

introducing an impurity into another region of the semiconductor by ion implantation using the gate electrode and the mask material as masks, to extend the another region under the gate electrode;

removing the mask material; and

introducing the impurity into the one region,

wherein the another region overlaps with the gate electrode more

widely than the one region overlaps with the gate electrode.

42. The method of claim 41 wherein the memory has a flash memory.

43. The method of claim 41 wherein the memory has an EPROM.

44. The method of claim 41 wherein the memory has an EEPROM.

45. A method for forming a MOS device comprising:

forming at least two gate electrode portions each having a floating gate on a semiconductor;

forming mask materials on at least two first regions of the semiconductor;

introducing an impurity into at least one second region of the semiconductor by ion implantation using the gate electrode portions and the mask materials, to extend the second region under the gate electrode portions;

removing the mask materials; and

introducing the impurity into the first regions,

wherein the second region overlaps with the gate electrode portions more widely than the first regions overlap with the gate electrode portions.

46. A method for forming a MOS device comprising:

forming at least two gate electrode portions each having a floating gate on a semiconductor;

forming mask materials on at least two first regions of the semiconductor;

introducing an impurity into at least one second region of the semiconductor by ion implantation using the gate electrode portions and the mask

materials, to extend the second region under the gate electrode portions;

removing the mask materials; and

introducing the impurity into the first regions, to form the first regions to a depth shallower than that of the second region.

47. The method of claim 46 wherein the first region each has 0.1 μm or less in depth.

48. The method of claim 46 wherein the second region overlaps with the gate electrode portions more widely than the first regions overlap with the gate electrode portions.

49. A method for forming MOS device comprising:

introducing an impurity into a semiconductor by ion implantation using at least two gate electrode portions each including a floating gate and a mask material as masks, to form at least one deep impurity region; and

introducing the impurity into the semiconductor using the gate electrode portions as masks, to form at least two shallow impurity region.

50. The method of claim 49 wherein the shallow impurity region each has 0.1 μm or less in depth.

51. The method of claim 49 wherein the deep impurity region extends under the gate electrode portions.

52. The method of claim 51 wherein the deep impurity region overlaps with the gate electrode portions more widely than the shallow impurity region overlap with the gate electrode portions.--